DATA SHEET

SUNPLUS

SP7021

Linux Computing Unit

2019-4-22

Preliminary 0.3

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SP7021 : A LINUX CHIP FOR IOT AND INDUSTRIAL CONTROL APPLICATIONS

"The power of Linux. The simplicity of a micro-controller."

SP7021 is a revolutionary SoC that has the power of a Linux-grade chip and the integration simplicity of a micro-controller.

Conceived by Sunplus Technology in collaboration with Tibbo Technology , SP7021 takes all the sophisticated elements typically found in modern industrial-grade embedded Linux chips, adds a plethora of features targeting IoT and industrial control applications, and delivers the resulting design in a simple microcontroller-like package that needs few external components, simplifies the schematic diagram, and reduces the PCB complexity.

1. Story

Although there are many embedded Linux CPUs on the market, few were designed to address the needs of the IoT and industrial control markets directly. In fact, most CPUs found on popular boards such as Raspberry Pi were initially meant for something else (for example, a SBC for education) and were merely repurposed for the needs of the IoT and industrial control communities.

Such CPUs usually have adequate processing power but lack in the IO features. This is not surprising, as set-top boxes have very different IO needs than IoT or industrial control devices. These CPUs are also rather complex, need multiple additional components to work, are available only in difficult-to-handle BGA packaging, and require six- or eight-layer boards. All these pose severe obstacles to low- and medium-volume device vendors.

Take the BGA packaging as an example. Everything about BGA is an order of magnitude more complex compared to other packaging choices, such as LQFP. BGA represents the cut-off line, at which it becomes impossible to handle the chips manually. Everything, from soldering to de-soldering, to verifying the assembly quality requires specialized and expensive equipment. Smartphone manufacturers accept BGA challenges as the inevitable side effect of the desired board miniaturization that BGA technology enables, but vendors of IoT or industrial control devices view this differently. IoT and industrial control products rarely have any size pressure, and having to deal with ever smaller IC packages only brings complications without any apparent benefit!

As another example, consider the logic levels of GPIO lines. As processor designs took advantage of more and more advanced fabrication processes, chip supply voltages have decreased too. With that, standard semiconductor IO libraries have dropped the support first for 5V, and then even for 3.3V logic levels. This did not bother the designers of set-top boxes and other "closed" products but was bad news for the architects of control hardware.

To summarize, there was an apparent gap between existing processor offerings and the requirements of the IoT and industrial control applications. Recognizing the unmet needs of IoT and industrial control vendors, in late 2017 Sunplus and Tibbo Technology have set out to develop a Linux-grade chip that would address these markets directly. The idea was to create a powerful SoC with IO features and packaging targeting specifically the IoT and the industrial control applications, as well as the needs of low- and medium-volume hardware manufacturers. Thus, the Plus1 concept was born.

Here are the key characteristics of the SP7021 SoC:

- Linux-grade system
- Single 3.3V power; integrated power controller and regulators for all additional voltages
- DRAM chip onboard
- Available simple-to-use LQFP packaging
- Flexible mapping of peripherals to chip pins
- 5V-tolerant 3.3V-level IO lines
- Dual Ethernet MAC controllers with the built-in Ethernet switch fabric
- Four enhanced UARTs as well as SPI/I2C, timers, PWM, and other peripherals
- Industrial operating temperature range (-40 ~ +85 C)
- Low EMI for simplified Class B CE/FCC certification
- Many more peripherals and features
- Robust ready-to-run modern Linux distribution available

1.GENERAL DESCRIPTION

SP7021 is a SoC solution of industrial control. It meets customers' full demand on function but with low cost so that will improve customers' competitiveness in the market. SP7021 provides rich GPIOs, storage and USB interface. And it provides MIPI CSI interface for video input and HDMI interface for video output. It also provides FPGA interface for function extension. SP7021 also has 4 Ethernet ports providing customers a high competitive solution.

2.FEATURES

2.1. Computation Power

- ARM Cortex-A7 Quad core
  - L1 cache: 32KB for data, 32KB for instruction
  - L2 cache: 512KB, 8 ways
  - Target frequency 960 MHz
  - AB IO using digital interface

2.2. SiP up to 512MB DDR3

- 64Mb/128Mb/256Mb * 16 DDR3 1066max (DDR3 KGD reach 1600)
- Need RDL to adjust pad location for bonding
- May need 5~10 pins for power / ground / DDR_ZQ)
- DRAM CTRL operating temperature : -40~85°C
- DDR3 KGD operating temperature : -20° ~ 85°C

2.3. Flash interface

- Support SPI NAND / SPI NOR / eMMC
- Support BCH ECC

2.4. Three separate MMC / SD / SDIO interfaces

- eMMC 4.41 DDR 104MB/s for primary boot disk
- SD card (SD 2.0) for second port removable media
- Third port SDIO (SD 2.0) interface for Wi-Fi module

2.5. GPIO

- 8-bit IO ports, total 9 ports
- Two ways of accessing individual GPIO lines
  - Through 8-bit registers, R/W at the same time
  - Individually, access single GPIO line without disturbing other lines in the same register
- Driving ability spec 16mA , only for GPIO0 port
- Separate interrupt configuration, 8 interrupt sources at GPIO1 port and need to be configure as wake-up source.
- 3.3V-logic GPIO lines with 5V tolerance
- Weak pull-ups with enable /open collector / invert in or out for GPIO1~GPIO8
- Weak pull-ups/Schmitt trigger /open collector / invert in or out for GPIO0
- Default pull-ups for all GPIO ports + all IOs as inputs
- The behavior of all boot-related pins is same as GPIO0
- All IO and peripherals also accessible by A926/8051

2.6. Two Ports Ethernet Switch

- 2 IEEE 802.3 10/100M ports
  - Dual 10/100 Ethernet MAC
  - Support RMII interface
  - Support half duplex and full duplex
  - Support full duplex flow control
  - Embedded IP/TCP checksum hardware accelerator
  - Programmable receiving maximum packet size(1536 bytes, 1522 bytes or 1518 bytes)
  - Programmable port default priority
- 2 SoC ports (with AHB interface)
  - Support frame transmission and receiving from/to CPU by SoC port
  - Support frame forwarding between SoC port and the other 2 ports
  - Programmable CRC padding by hardware or software
  - Programmable SoC port MAC address and VLAN group
  - Descriptor based control/status exchange between CPU and the switch hardware
  - Embedded data/descriptor DMA engine
  - Programmable port default priority

- Independent MAC address for independent driver
- VLAN
  - Support IEEE802.1Q VLAN tagging and un-tagging
  - Programmable default VLAN group for each port
  - Programmable 16 VLAN groups and member sets of each VLAN group
  - Support VLAN priority
- Address Table
  - 1K MAC address table entries
  - MAC address table programmable by CPU
  - Support MAC clone and MAC security
  - MAC address table addressing mode: direct or hash base on MAC address
  - Programmable aging time
- Quality of Service (QoS)
  - Support 4 traffic class (compatible with IEEE802.1D-2004)
- System Interface
  - 32-bit AHB master interface as DMA bus
  - 32-bit AHB slave interface as register configuration bus
- MISC
  - Provide control lines for status LEDs("link up/down" and "100M/10M")
  - Fully independent and connected to two independent LAN segments
  - Only one of the MACs is accessible from the CPU
  - Support 2 operation modes : NIC and Daisy Chain mode
  - Handle pass-through Ethernet traffic without any CPU intervention

2.7. Five UARTs

- One console UART with only Tx/Rx lines
- Four full function UART
  - Large FIFOs, 128 bytes depths
  - Enhanced UARTs with automatic RTS/CTS control
  - Clocking each UART from 27MHz or one CLK input
- Baud rate 921600 with Error rate under 3%
- Each port with independent Tx/Rx DMA function

2.8. Four SPI_Combo(Master/Slave) and Four I2C(Master Only)

- I2C clock stretching and buffer depth FIFO 32
- SPI buffer depth FIFO 8 of RX and TX registers
- Each port with independent Tx/Rx DMA function

2.9. PWM, Timers, input capture module

- PWM : Two independent modules
  - Each module contain at least four synchronized PWM channels
  - More than 70MHz PWM resolution
- Four General Purpose Timers :
  - Four 8b and up to two 16b timers/counters
- Four Input Capture (IC) module
- Independent Watchdog Timer (WDT)

2.10. Security Boot

- Secure boot verified by ED25519 algorithm
- External image will be verified signature by fixed ROM code with internal OTP public key before the operating system has been loaded.

2.11. Crypto Engine

- PKA Engine (RSA)
- Hash Engine (SHA3, MD5)
- Bulk Encryption/decryption Engine (AES)

2.12. RTC

- Standby mode definition : sustain more than one year with 250mAH battery.
- RTC with leap year and daylight saving time correction with software library support
- RTC with alarm timer with its own output port
  - CPU set the wakeup time, shutdown until this time

- RTC wake up port to output pin and CPU interrupt
- RTC connect to the backup power pin, charging battery without adding any charging circuit

2.13. Two USB interfaces

- High-speed USB 2.0 IP
- Both ports support OTG and integrated PHY
- Need boot from each USB port
- Support USB video class (UVC).

2.14. SWD interface

- Dedicated pins for easy debug
- Pin mux with other function for other product

2.15. Unique factory info and OTP memory

- IC Vendor （before shipping）
  - Device ID, revision, 16b
  - The serial number (unique ID, can be MAC address ?)
  - Two “registered” MAC addresses for two MAC controllers (each 48b)
- User :
  - 64 bytes of one-time programmable memory for storing user IDs, hash data(for protection)
- HDCP key 384 bytes for HDMI 1.4 Tx
- Total 512 bytes
- Without extra hardware to program OTP, with extra OTP program voltage pin

2.16. Pin Mux

- Any signals of each function could map to any pin using pin mux mapping matrix
- Program after reset by register and during Linux operation

2.17. SPI-FLASH controller

- Support 1 bit/ 2bits/4-bits SPI_FLASH memory

2.18. MIPI CSI

- Support two CSI-RX modules, both CSI-RX modules have following features.
- Compliant with the MIPI CSI-2 Specification ,rev 1.01 and MIPI D-PHY interface Specification, version1.1
- HS (high speed), LP (low power) mode supported
- 10Mbps per lane in low power mode
- Support Power-down mode
- Support MIPI CSI-2 short and long packet formats
- Per lane support up to 1.0 Gbps
- Support MIPI CSI-2 1 data lane
- Total bandwidth required : 810 Mbps
- Support MIPI CSI-2 data format: RAW8, RAW10
- Image Interface to core processor : 10 bits
- Color depth / Bits per pixel : 10 bits per pixels
- Configuration Interface to core processor : APB
- Support CCI or I2C master for Camera Control Interface
- Camera pixel resolution : 1328x864 (Include non-image data)
- Frames per second : 60 FPS
- Virtual Channel : No need

2.19. Simple version LCD Timing Controller (TCON)

- Support TTL interface panel for monitor, resolution 320x240.
- Support TTL RGB888 output

2.20. Others

- A926 200MHz with 16KB I/D cache
  - For test without computation unit
  - Run as RPU when production
- IOP MCU, 8051
  - For standby mode operation
  - Standby mode power spec 400uA
- Boot up time 5 sec
- DMA accelerator
- HDMI 1.4 Tx for still image terminal, resolution up to 720P
- Camera, video and audio interfaces
  - Camera :
    - MIPI camera : for light application without ISP
    - USB camera : support USB video class (UVC)

- Video :
  - MIPI data fetch with de-bayering engine
  - 1 layer OSD (on screen display) with 8 bit indexed color (RGBA)
  - Display mixer
  - Resolution up to 1366X768 and 1312X816
- Audio :
  - I2S output up to 5 stereo channel
  - I2S input up to 4 stereo channel
  - SPDIF output up to 1 spdif output
  - SPDIF input up to 1 spdif input
  - Support PDM interface for MEMS microphone 8 channel
  - PCM (TDM/I2S ifx, 1-Rx+1-Tx ifx)
    - TDM support 16/24/32b 8 channel , master /slave mode
  - Digital audio PWM output up to 2 channel , each have 4 PWMs output
- Temperature sensor embedded (resolution 1°C), for chip operation temperature detection (temperature detection range - 40°C ~ 125°C)
- Embedded DC-DC for computation unit , DDR3, core power
  - Computation unit 700mA at 3.3 to 0.86V (from A chip system spec 0.86V 125°), under +-5% voltage variation
  - DDR3 supply 350mA at 3.3 to 1.5V (Micron DDR3 at 1600 is 300mW), under +-5% voltage variation
  - B chip core power 800mA at 3.3 to 1.2V, under +-5% voltage variation
  - Robust power sequence power good, only single 3.3 power supply
- FCC Class B for system level, Industrial temperature range - 40°C ~ 85°C
- 20X20 LQFP176 pins, 2L/4L PCB
- Working power : < 2W at 85°C

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3.SYSTEM DIAGRAM

3.1. SP7021

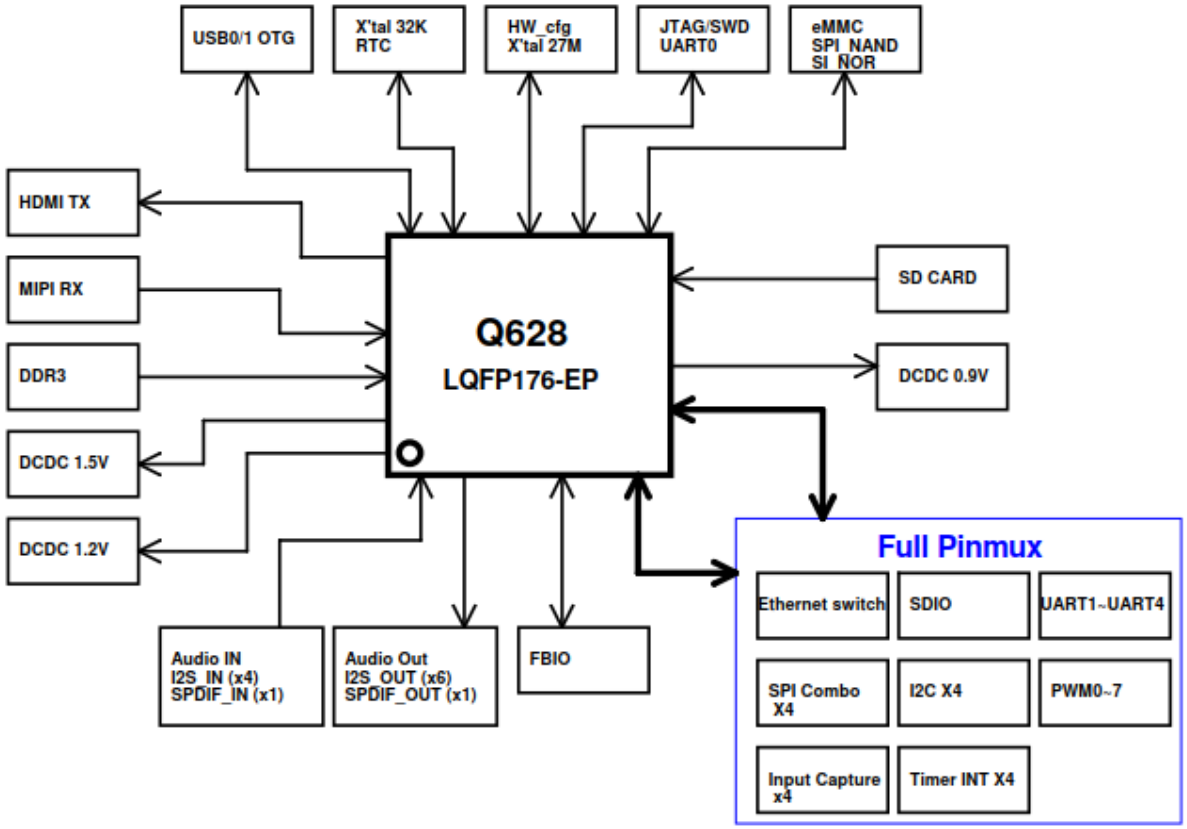

Figure 1. System Block

4.BLOCK DIAGRAM

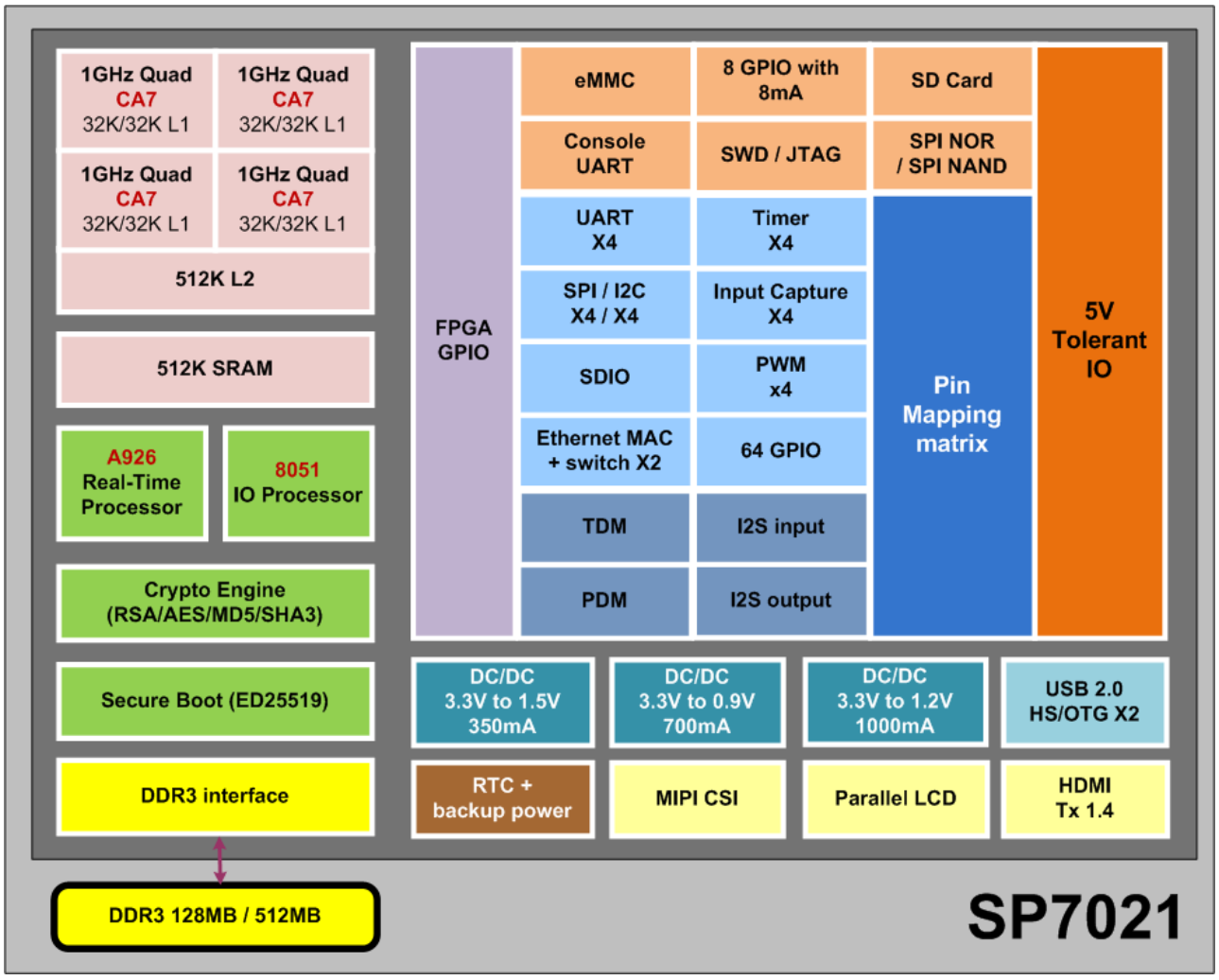

Figure 2. Function Block

5.SIGNAL DESCRIPTIONS

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5.1. SP7021 Pin Assignment

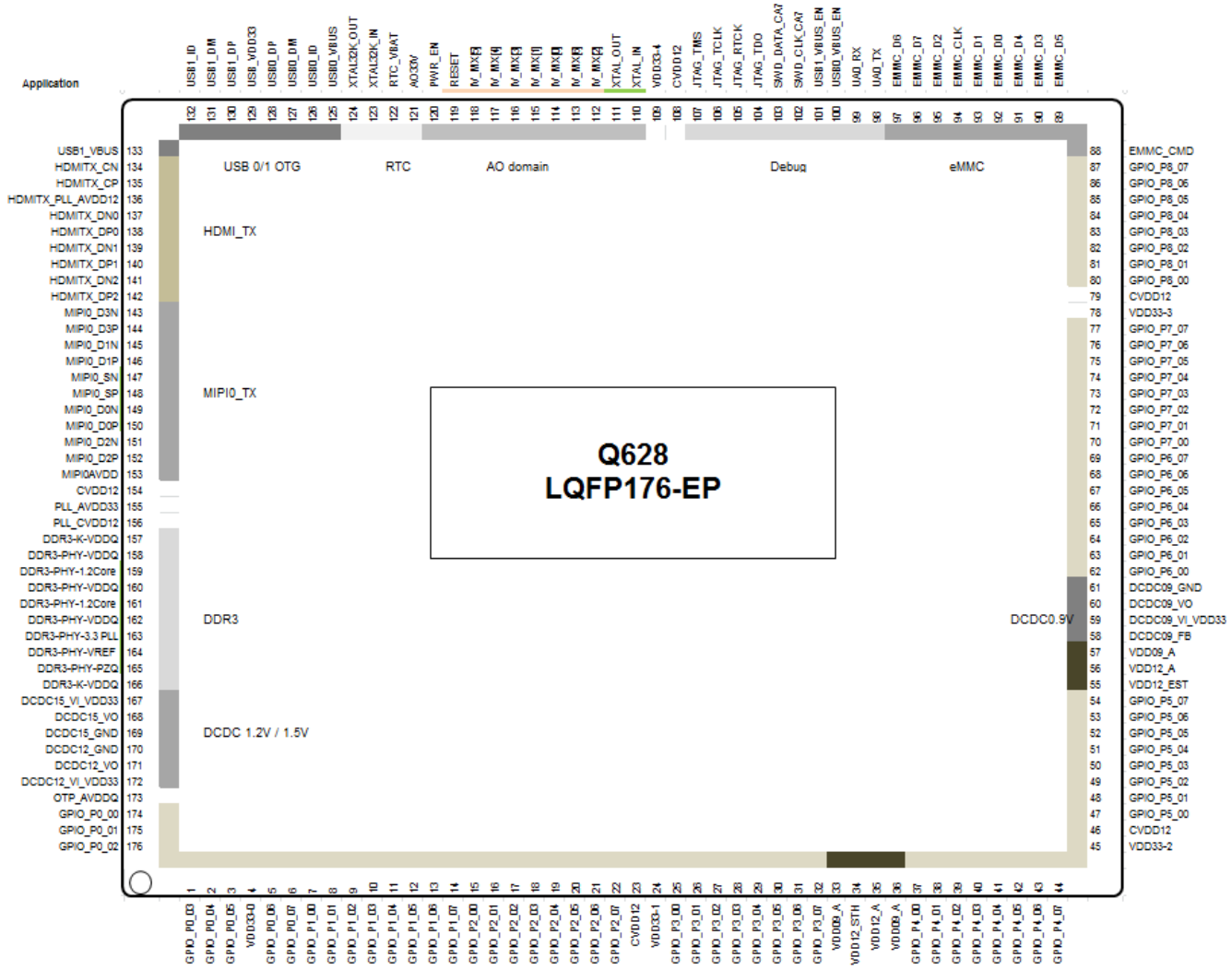


Figure 3. Pin Assignment

5.2. SP7021 Pin Description

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
GPIO_P0_03	1	I/O		UPHY1_I2C_SDA	GPIO03	General purpose I/O or FPGA I/O or USBPHY1 I2C SDA
GPIO_P0_04	2	I/O		UPHY0_I2C_SCL	GPIO04	General purpose I/O or FPGA I/O or USBPHY0 I2C SCL
GPIO_P0_05	3	I/O		UPHY0_I2C_SDA	GPIO05	General purpose I/O or FPGA I/O or USBPHY0 I2C SDA
B_ForGPIO_VDD33_0	4	S				I/O power supply pins
GPIO_P0_06	5	I/O		UPHY1_I2C_SCL	GPIO06	General purpose I/O or FPGA I/O or USBPHY2 I2C SCL
GPIO_P0_07	6	I/O		UPHY1_I2C_SDA	GPIO07	General purpose I/O or FPGA I/O or USBPHY2 I2C SDA
GPIO_P1_00	7	I/O		I2S_IN_MCK	GPIO08	General purpose I/O or FPGA I/O or I2S_IN_MCK
GPIO_P1_01	8	I/O		I2S_IN_BCK	GPIO09	General purpose I/O or FPGA I/O or I2S_IN_BCK
GPIO_P1_02	9	I/O		I2S_IN_LRCK	GPIO10	General purpose I/O or FPGA I/O or I2S_IN_LRCK
GPIO_P1_03	10	I/O		I2S_IN_D0	GPIO11	General purpose I/O or FPGA I/O or I2S_IN_D0
GPIO_P1_04	11	I/O		I2S_IN_D1	GPIO12	General purpose I/O or FPGA I/O or I2S_IN_D1
GPIO_P1_05	12	I/O		I2S_IN_D2	GPIO13	General purpose I/O or FPGA I/O or I2S_IN_D2
GPIO_P1_06	13	I/O		I2S_IN_D3	GPIO14	General purpose I/O or FPGA I/O or I2S_IN_D3
GPIO_P1_07	14	I/O		PDM_IN_CLK_OUT/ TDM_IN_CLK	GPIO15	General purpose I/O or FPGA I/O or PDM_IN_CLK_OUT or TDM_IN_CLK
GPIO_P2_00	15	I/O		PDM_IN_CLK_D0/ TDM_IN_SYNC	GPIO16	General purpose I/O or FPGA I/O or PDM_IN_D0 or TMD_IN_SYNC or UA4AXI_TXD
GPIO_P2_01	16	I/O		PDM_IN_CLK_D1/ TDM_IN_DATA4	GPIO17	General purpose I/O or FPGA I/O or PDM_IN_D1 or TMD_IN_DATA4 or UA4AXI_RXD
GPIO_P2_02	17	I/O		PDM_IN_CLK_D2/ TDM_IN_DATA8	GPIO18	General purpose I/O or FPGA I/O or PDM_IN_D2 or TMD_IN_DATA8 or UA4AXI_RST
GPIO_P2_03	18	I/O		PDM_IN_CLK	GPIO19	General purpose I/O or FPGA I/O

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
				_D3		or PDM_IN_CLK_D3
GPIO_P2_04	19	I/O		SPDIF_IN	GPIO20	General purpose I/O or FPGA I/O or SPDIF_IN
GPIO_P2_05	20	I/O		I2S_OUT_MCK/ TDM_OUT_MCK	GPIO21	General purpose I/O or FPGA I/O or I2S_OUT_MCK/ TDM_OUT_MCK
GPIO_P2_06	21	I/O		I2S_OUT_BCK/TDM_OUT_BCK	GPIO22	General purpose I/O or FPGA I/O or I2S_OUT_BCK/ TDM_OUT_BCK
GPIO_P2_07	22	I/O		I2S_OUT_LRCK/TDM_OUT_SYNC	GPIO23	General purpose I/O or FPGA I/O or I2S_OUT_LRCK/ TDM_OUT_SYNC
CVDD12	23	S				Core power 1.2V
B_ForGPIO_VDD33_1	24	S				I/O power supply pins
GPIO_P3_00	25	I/O		I2S_OUT_D0/ TDM_OUT_DATA4	GPIO24	General purpose I/O or FPGA I/O or I2S_OUT_D0 or TDM_OUT_DATA4
GPIO_P3_01	26	I/O		I2S_OUT_D1/ TDM_OUT_DATA8	GPIO25	General purpose I/O or FPGA I/O or I2S_OUT_D1 or TDM_OUT_DATA8
GPIO_P3_02	27	I/O		I2S_OUT_D2/ TDM_OUT_DATA16	GPIO26	General purpose I/O or FPGA I/O or I2S_OUT_D2 or TDM_OUT_DATA16
GPIO_P3_03	28	I/O		I2S_OUT_D3	GPIO27	General purpose I/O or FPGA I/O or I2S_OUT_D3
GPIO_P3_04	29	I/O		I2S_OUT_D4	GPIO28	General purpose I/O or FPGA I/O or I2S_OUT_D4
GPIO_P3_05	30	I/O		I2S_OUT_D5	GPIO29	General purpose I/O or FPGA I/O or I2S_OUT_D5
GPIO_P3_06	31	I/O		SPDIF_OUT	GPIO30	General purpose I/O or FPGA I/O or SPDIF_OUT
GPIO_P3_07	32	I/O		FPGA_PAD31	GPIO31	General purpose I/O or FPGA I/O
VDD09_A	33	S				0.9V core power for A-chip
VDD12_STH	34	S				
VDD12_A	35	S	HW_CFG[3]			1.2V core power for A-chip
VDD09_A	36	S	HW_CFG[2]			0.9V core power for A-chip
GPIO_P4_00	37	I/O		FPGA_PAD32	GPIO32	General purpose I/O or FPGA I/O
GPIO_P4_01	38	I/O		FPGA_PAD33	GPIO33	General purpose I/O or FPGA I/O

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
GPIO_P4_02	39	I/O		FPGA_PAD34	GPIO34	General purpose I/O or FPGA I/O
GPIO_P4_03	40	I/O		FPGA_PAD35	GPIO35	General purpose I/O or FPGA I/O
GPIO_P4_04	41	I/O		FPGA_PAD36	GPIO36	General purpose I/O or FPGA I/O
GPIO_P4_05	42	I/O		FPGA_PAD37	GPIO37	General purpose I/O or FPGA I/O
GPIO_P4_06	43	I/O		FPGA_PAD38	GPIO38	General purpose I/O or FPGA I/O
GPIO_P4_07	44	I/O		FPGA_PAD39	GPIO39	General purpose I/O or FPGA I/O
B_ForGPIO_VDD33_2	45	S				I/O power supply pins
CVDD12	46	S				1.2V core power
GPIO_P5_00	47	I/O		FPGA_PIN40	GPIO40	General purpose I/O or FPGA I/O
GPIO_P5_01	48	I/O		FPGA_PIN41	GPIO41	General purpose I/O or FPGA I/O
GPIO_P5_02	49	I/O		FPGA_PIN42	GPIO42	General purpose I/O or FPGA I/O
GPIO_P5_03	50	I/O		FPGA_PIN43	GPIO43	General purpose I/O or FPGA I/O
GPIO_P5_04	51	I/O		FPGA_PIN44	GPIO44	General purpose I/O or FPGA I/O
GPIO_P5_05	52	I/O		FPGA_PIN45	GPIO45	General purpose I/O or FPGA I/O
GPIO_P5_06	53	I/O		FPGA_PIN46	GPIO46	General purpose I/O or FPGA I/O
GPIO_P5_07	54	I/O		FPGA_PIN47	GPIO47	General purpose I/O or FPGA I/O
VDD12_EST	55	S				
VDD12_A	56	S				1.2V power supply
VDD09_A	57	S				
DCDC09_FB	58	S				DCDC-09 Feedback voltage
DCDC09_VI_VDD33	59	S				DCDC-09 3.3V power input
DCDC09_VO	60	S				DCDC-09 power output
DCDC09_GND	61	S				DCDC-09 Ground
GPIO_P6_00	62	I/O		GPIO_P6_00	GPIO48	General purpose I/O
GPIO_P6_01	63	I/O		GPIO_P6_01	GPIO49	General purpose I/O

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
GPIO_P6_02	64	I/O		JTAG_TRST	GPIO50	General purpose I/O or JTAG TRST
GPIO_P6_03	65	I/O		JTAG_TMS	GPIO51	General purpose I/O or JTAG TMS
GPIO_P6_04	66	I/O		JTAG_TCK	GPIO52	General purpose I/O or JTAG TCK
GPIO_P6_05	67	I/O		JTAG_TDI	GPIO53	General purpose I/O or JTAG TDI
GPIO_P6_06	68	I/O		JTAG_TDO	GPIO54	General purpose I/O or JTAG TDO
GPIO_P6_07	69	I/O		JTAG_RTCK	GPIO55	General purpose I/O or JTAG RTCK
GPIO_P7_00	70	I/O		GPIO_P7_00	GPIO56	General purpose I/O
GPIO_P7_01	71	I/O		SWD_CLK	GPIO57	General purpose I/O or SWD CLK
GPIO_P7_02	72	I/O		SWD_DATA	GPIO58	General purpose I/O or SWD DATA
GPIO_P7_03	73	I/O		GPIO P7_03	GPIO59	General purpose I/O
GPIO_P7_04	74	I/O		GPIO P7_04	GPIO60	General purpose I/O
GPIO_P7_05	75	I/O		GPIO P7_05	GPIO61	General purpose I/O
GPIO_P7_06	76	I/O		HDMITX_SDA	GPIO62	General purpose I/O or HDMXTX SDA
GPIO_P7_07	77	I/O		HDMITX_SCL	GPIO63	General purpose I/O or HDMITX SCL
B_ForGPIO_VDD33_3	78	S				I/O power supply pins
CVDD12	79	S				1.2V core power
GPIO_P8_00	80	I/O		SD_SENSE	GPIO64	General purpose I/O or SD Card Sense
GPIO_P8_01	81	I/O		SD_D1	GPIO65	General purpose I/O or SD Card D1
GPIO_P8_02	82	I/O		SD_D0	GPIO66	General purpose I/O or SD Card D0
GPIO_P8_03	83	I/O		SD_CLK	GPIO67	General purpose I/O or SD Card CLK
GPIO_P8_04	84	I/O		SD_CMD	GPIO68	General purpose I/O or SD Card CMD
GPIO_P8_05	85	I/O		SD_D3	GPIO69	General purpose I/O or SD Card D3
GPIO_P8_06	86	I/O		SD_D2	GPIO70	General purpose I/O or SD Card D2
GPIO_P8_07	87	I/O		GPIO P8_07	GPIO71	General purpose I/O
EMMC_CMD	88	I/O		EMMC_CMD	GPIO72	General purpose I/O or EMMC

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
						CMD
EMMC_D5	89	I/O		EMMC_D5	GPIO73	General purpose I/O or EMMC D5
EMMC_D3	90	I/O		EMMC_D3	GPIO74	General purpose I/O or EMMC D3
EMMC_D4	91	I/O		EMMC_D4	GPIO75	General purpose I/O or EMMC D4
EMMC_D0	92	I/O		EMMC_D0	GPIO76	General purpose I/O or EMMC D0
EMMC_D1	93	I/O		EMMC_D1	GPIO77	General purpose I/O or EMMC D1
EMMC_CLK	94	I/O		EMMC_CLK	GPIO78	General purpose I/O or EMMC CLK
EMMC_D2	95	I/O		EMMC_D2	GPIO79	General purpose I/O or EMMC D2
EMMC_D7	96	I/O		EMMC_D7	GPIO80	General purpose I/O or EMMC D7
EMMC_D6	97	I/O		EMMC_D6	GPIO81	General purpose I/O or EMMC D6
UA0_TX	98	I/O		UA0_TX	GPIO88	General purpose I/O or UA0 Tx
UA0_RX	99	I/O		UA0_RX	GPIO89	General purpose I/O or UA0 RX
USB0_VBUS_EN	100	I		USB0_VBUS_EN	GPIO90	General purpose I/O or USB0 VBUS Enable
USB1_VBSU_EN	101	I		USB1_VBSU_EN	GPIO91	General purpose I/O or USB1 VBUS Enable
SWD_CLK	102	I/O		SWD_CLK	GPIO82	General purpose I/O or SWD CLK
SWD_DAT	103	I/O		SWD_DAT	GPIO83	General purpose I/O or SWD DATA
JTAG_TDO	104	I/O		JTAG_TDO	GPIO84	General purpose I/O or JTAG TDO
JTAG_RTCK	105	I/O		JTAG_RTCK	GPIO85	General purpose I/O or JTAG RTCK
JTAG_TCK	106	I/O		JTAG_TCK	GPIO86	General purpose I/O or JTAG TCK
JTAG_TMS	107	I/O		JTAG_TMS	GPIO87	General purpose I/O or JTAG TMS
CVDD12	108	S				DDR PLL Power 1.2V
B_ForGPIO_VDD33_4	109	S				SSTL reference voltage
XTAL_IN	110	I	HW_CFG[5]	XTALI		27MHz Crystal PAD input
XTAL_OUT	111	I		XTALO		27MHz Crystal PAD output
JTAG_TDI	112	I/O			GPIO98	General purpose I/O or JTAG TDI
JTAG_TRST	113	I/O			GPIO97	General purpose I/O or JTAG TRST
IV_MX0	114	I/O			GPIO92	General purpose I/O
WakeUp/IV_MX1	115	I/O	HW_CFG[0]		GPIO93	General purpose I/O or Wakeup or HW_CFG pin at reset
IV_MX3	116	I/O	HW_CFG[1]		GPIO94	General purpose I/O or HW_CFG pin at reset

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
IV_MX4	117	I/O	HW_CFG[2]		GPIO95	General purpose I/O or HW_CFG pin at reset
IV_MX5	118	I/O	HW_CFG[3]		GPIO96	General purpose I/O or HW_CFG pin at reset
RESET	119	I/O			GPIO4	System Reset
PWR_EN	120	I/O			GPIO5	Power enable output pin
AO33V	121	S			GPIO6	3.3V power for AO domain
RTC_VBAT	122	S				Battery supply voltage
XTAL32K_IN	123	I/O		XTAL32K_IN		32KHz Crystal PAD input
XTAL32K_OUT	124	I/O		XTAL32K_OUT		32KHz Crystal PAD output
USB0_VBUS	125	I				USB0 VBUS
USB0_ID	126	I/O				USB0 ID
USB0_DM	127	I/O				USB0 bus D-
USB0_DP	128	I/O				USB0 bus D+
USB_VDD33	129	S				3.3V power for USB PLL and USB transceiver
USB1_DP	130	I/O				USB1 bus D-
USB1_DM	131	I/O				USB1 bus D+
USB1_ID	132	I/O				USB1 ID
USB1_VBUS	133	S				USB1 VBUS
HDMITX_CN	134	I/O				HDMITX Clock-
HDMITX_CP	135	I/O				HDMITX Clock+
HDMITX_PLL_AVDD12	136	S				HDMITX PLL 1.2V power
HDMITX_DN0	137	I/O				HDMITX Data0-
HDMITX_DP0	138	I/O				HDMITX Data0+
HDMITX_DN1	139	I/O				HDMITX Data1-
HDMITX_DP1	140	I/O				HDMITX Data1+
HDMITX_DN2	141	I/O				HDMITX Data2-
HDMITX_DP2	142	I/O				HDMITX Data2+
MIPI_D3N	143	I/O				MIPI Data3-
MIPI_D3P	144	I/O				MIPI Data3+
MIPI_D1N	145	I/O				MIPI Data1-
MIPI_D1P	146	I/O				MIPI Data1+
MIPI_SN	147	I/O				MIPI Clock-
MIPI_SP	148	I/O				MIPI Clock+
MIPI_D0N	149	I/O				MIPI Data0-

Pin Name	Pin No	Type	Symbol			Description
			HW_CFG	Normal Function	GPIO	
MIPI_D0P	150	I/O				MIPI Data0+
MIPI_D2N	151	I/O				MIPI Data2-
MIPI_D2P	152	I/O				MIPI Data2+
MIPIAVDD	153					MIPI 1.2V power
CVDD12	154					1.2V core power
PLL_AVDD33	155					PLL 3.3V power
PLL_CVDD12	156	S				PLL 1.2V power
DDR3-K-VDDQ	157	S				DDR3 KGD IO power
DDR3-PHY-VDDQ	158	S				DDR3-PHY IO power
DDR3-PHY-12Core	159	S				DDR3-PHY core power
DDR3-PHY-VDDQ	160	S				DDR3-PHY IO power
DDR3-PHY-1.2Core	161	S				DDR3-PHY core power
DDR3-PHY-VDDQ	162	S				DDR3-PHY IO power
DDR3-PHY-3.3PLL	163	S				DDR3-PHY PLL power
DDR3-PHY-VREF	164	S				DDR3-PHY reference voltage
DDR3-PHY-PZQ	165	S				DDR3-PHY external reference resistor
DDR3-K-VDDQ	166	S				DDR3 KGD IO power
DCDC15_VI_VDD33	167	S				DCDC-15 3.3V power input
DCDC15_VO	168	S				DCDC-15 power output
DCDC15_GND	169	S				DCDC-15 Ground
DCDC12_GND	170	S				DCDC-12 Ground
DCDC12_VO	171	S				DCDC-12 power output
DCDC12_VI_VDD33	172	S				DCDC-12 3.3V power input
OTP_AVDDQ	173	S				OTP VDDQ power
GPIO_P0_00	174	I/O				General purpose I/O or FPGA I/O
GPIO_P0_01	175	I/O				General purpose I/O or FPGA I/O
GPIO_P0_02	176	I/O				General purpose I/O or FPGA I/O

Note: “I/O” means bidirectional input/output pin. “S” means power/ground pin. “A” means analog pin. “I” means input pin. “O” means output pin.

6.FUNCTIONAL DESCRIPTIONS

6.1. SPI NOR

The SPI_NOR Controller is used to transmit or receive data with SPI_NOR device. Support 1/2/4 bit transferred mode.

- Support 1 byte length or skip command bits
- Address Bytes
  Support 1/2/4 bit transferred mode
  Support 1/2/3 byte length or skip address bits
- Support 2/4/6/8/16/32 dummy cycles or skip dummy cycles
- Data Bytes
  Support 1/2/4 bit transferred mode
  Support 1 - 65535 byte length or skip

6.2. SPI NAND

SPI_NAND Controller is used to transmit or receive data with SPI_NAND device.

- Command Byte
  Support 1/2/4 bit transferred mode
  Support 1 byte length or skip command bits
- Address Bytes
  Support 1/2/4 bit transferred mode
  Support 1/2/3 byte length or skip address bits
- Support 2/4/6/8/16/32 dummy cycles or skip dummy cycles
- Data Bytes
  Support 1/2/4 bit transferred mode
  Support 1 - 65535 byte length or skip data bits
- SPI Device Number
  Support 1 or 2 SPI chips
- Support configurable chip selected, command should be valid only relative chip selected.
- Support BCH auto encode and decode
- Support 32-bit AXI master bus for transferring data between controller and dram for DMA mode
- Exchange to 32-bit AXI Slave bus from 32-bit OCP bus
- Support auto multi page read
- Support auto multi page program
- Support enable BCH function for DMA mode
- Support SPI_CLK is divided from CLK_SPI, and frequency division coefficient is 1/2, 1/4, 1/6, 1/8, 1/16, 1/24, 1/32

6.3. eMMC

- eMMC controller, used for primary boot disk, support emmc 4.41 DDR 104MB/s speed mode.
- EMMC Speed Mode
  - Default speed(26MHz)
  - High speed SDR mode(52MHz)
  - High speed DDR mode(52MHz)
- Support Card Bit Mode
  - 1 bit、4 bit、8 bit
- Support Timing Adjustment
  - clock auto adjustment
  - write auto adjustment
  - read auto adjustment
- Support Data Transfer Mode
  - EMMC PIO/DMA/HW DMA mode
  - Single/Multiple block read/write

6.4. SDIO

The SDIO controller, used for Wi-Fi module, supports SDIO 2.0 SDR 25MB/s speed mode.

- Support SDIO 2.0
- Support Card Capacity
  - Support SDHC and SDXC
- Support Card Speed Mode
- SDIO Speed Mode

- Support Default speed(25MHz)
- Support High speed SDR mode(50MHz)

- Support Card Bit Mode
  - Support 1 bit、4 bit
- Support Timing Adjustment
  - Support clock auto adjustment
  - Support write auto adjustment
  - Support read auto adjustment
  - Adjustment range is 1~7 DPLL clock cycle
- Support Data Transfer Mode
  - Support SDIO/SD PIO/DMA mode
  - Support Single/Multiple block read/write

6.5. SD Card

The SD controller, used for removable media, supports SD 2.0 SDR 25MB/s speed mode.

- Support SD 2.0
- Support Card Capacity
  - Support SDHC and SDXC
- SDIO/SD Speed Mode
  - Support Default speed(25MHz)
  - Support High speed SDR mode(50MHz)
- Support Card Bit Mode
  - Support 1 bit、4 bit
- Support Timing Adjustment
  - Support clock auto adjustment
  - Support write auto adjustment
  - Support read auto adjustment
- Support Data Transfer Mode
  - Support SDIO/SD PIO/DMA mode
  - Support Single/Multiple block read/write

6.6. SPI Combo

The SPI is Serial Peripheral Interface Bus, similar to I²C, is a 4-wire synchronous serial data protocol for portable device platform systems. The existing SPI master IP can only be one-way transmission (slave to master). Add the path from master to slave.

6.7. I2C

The I2C MASTER has the follows function:

- Support Standard-mode and Fast-mode
- Buffer depth FIFO 32
- Support Read Mode, Write Mode and Restart Mode
- Support clock stretching
- Support DMA function

6.8. UART

UART is a peripheral IP, the interface is EIA RS-232C DB-9.

Transmitting and receiving data at the same time.

FIFO depth can be defined:

128byte / 64byte / 16byte / 4byte.

The internal loop-back capability allows on-board diagnostics.

6.9. Input Capture

The Input Capture module (ICM) is used to capture a counter value from the ICM's internal counter based upon an event on an input pin. The ICM features are useful in applications that require frequency (time period) and pulse measurement.

The ICM includes four sub module and the detail features of the sub module as below.

- 5 to 1 input signal MUX. 4 external input signal and 1 internal test signal. Test signal generate from system clock and support to scale the period.
- One de-bounce filter
- Three operating modes and all of them can set event times that decide when to trigger interrupt.
  - Rising Edge Detect Mode
  - Falling Edge Detect Mode
  - Edge Detect Mode
- Report pulse width (high and low) for pulse measurement

- A FIFO buffer (depth is 16) which can record 16 times counter value. User can read from register and the FIFO counter will decrease one. If FIFO is full, the new counter value will be discarded.

6.10. Audio IN

Audio IN interface contains the standard I2S and S/PDIF interface, signal recording form ADC, and multi-channel mix. It supports up to192KHz sample rate. It also can decode the I2s or S/PDIF signal and save the data in DRAM for further usage. The input path is shown as figure 4.

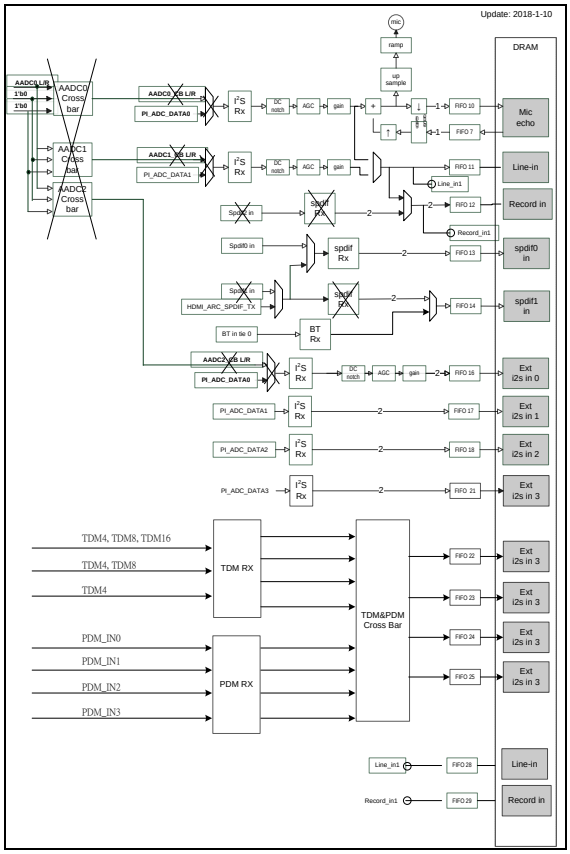


Figure 4: Audio In Diagram

6.11. Audio Out

When the audio data has been decoded by DSP and saved in DRAM, Audio module will fetch the data from DRAM and encode it with I2S or S/PDIF protocol, and the output path is shown as figure 5.

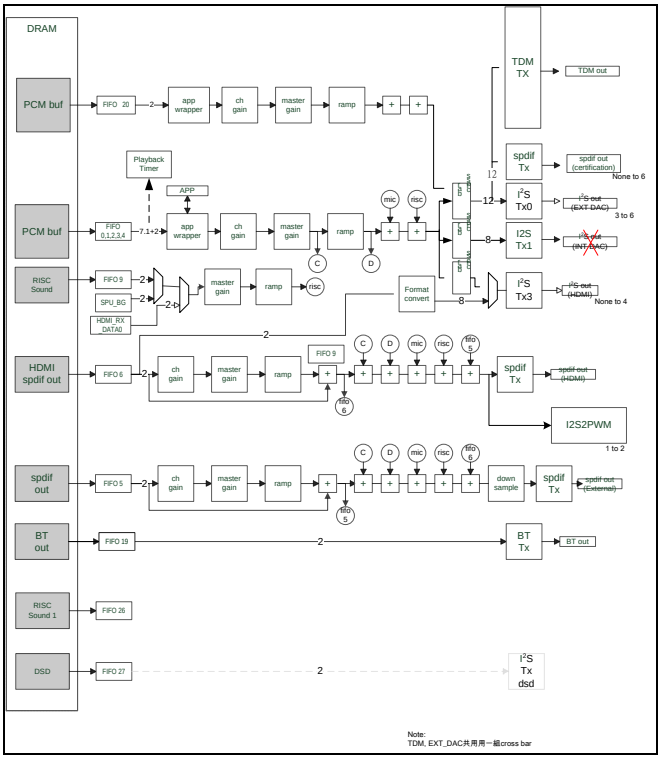


Figure 5: Audio Output Diagram

6.12. Simple version LCD Timing Controller (TCON)

TTL interface timing supports 320x240 and RGB888 outputs, 2 simple functions, RGB side reverse and RGB channel switching.

6.13. HDMI TX

HDMI is stand for "High Definition Multimedia Interface" to transmit high quality video and audio in a single cable. This HDMI Tx IP is composed of video, audio and HDCP cipher engine and intends to be integrated to a SoC to deliver high quality video and audio over a single cable.

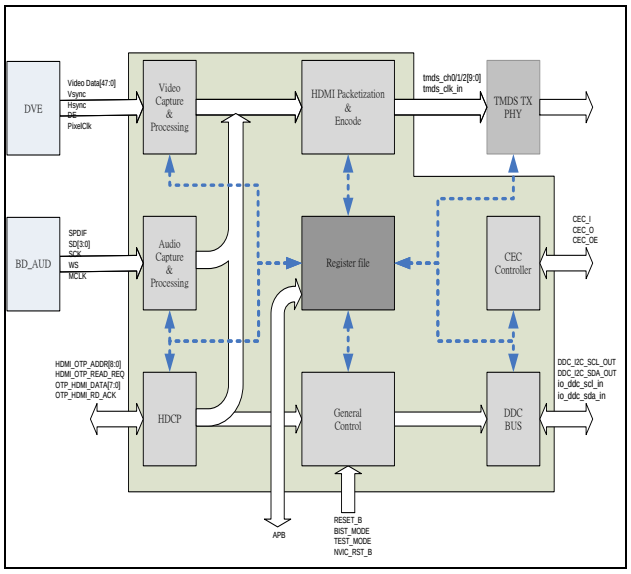


Figure 6: HDMI Block Diagram

7. ELECTRICAL CHARACTERISTICS

7.1. Absolute Maximum Ratings

Symbol	Parameter	MIN.	MAX.	Unit
V_{DVD33}, V_{VDD33_AO}	Supply voltage 3.3V	-0.3	3.45	V
V_{DVDD12}	Supply voltage 1.2V	-0.3	1.25	V
V_{CVDD09}	Supply voltage 0.9V	-0.3	0.945	V
V_O	Output voltage	-0.3	V_{DVD33} + 0.3	V
V_i	Input voltage (non 5V tolerant inputs) (#1)	-0.3	V_{DVD33} + 0.3	V
V_{i5vtol}	Input voltage (5V tolerant inputs) (#2)	-0.3	5.5	V
T_{J-MAX}	Junction temperature		125	°C
T_{STG}	Storage temperature	-55	150	°C
T_{SOL}	Lead temperature (soldering, 4 sec)		260	°C

Note:

7.2. Thermal Information

Symbol	Parameter	Unit(°C/W)
Θ_{JA}	Thermal resistance, junction to ambient(4 Layer PCB), Ambient 70°C	25.17
Ψ_{JT}	Junction-to-top characterization parameter	1.44

Note: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In application where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.3. ESD Ratings

Symbol	Parameter	Value		Unit
V_{ESD}	Human Body Model (test Per JESD22-A114F, Class 2)			KV
	Machine Model (test Per JESD22-A115C, Class B) (Note 1)			V
	Charge Device Model (test per JESD22-C101E, Class III)			V
I_{LA}	Latch-up tolerance (test Per JESD78C, Class I)			mA

Note 1:

7.4. DC Operating Conditions

Voltage referenced to VSS=0V, T_{OPT} =0°C to 70°C

Symbol	Parameter	MIN.	Nom.	MAX.	Unit
V_{DVD33}, V_{VDD33_AO}	Supply voltage 3.3V	3.15	3.3	3.45	V
V_{DVDD18}	Supply voltage 1.8V	1.62	1.8	1.98	V
V_{CVDD12}	Supply voltage 1.2V	1.15	1.2	1.25	V
T_J	Operating Junction temperature			105	°C
T_{OPT}	Operating temperature	0		70	°C

Note:.

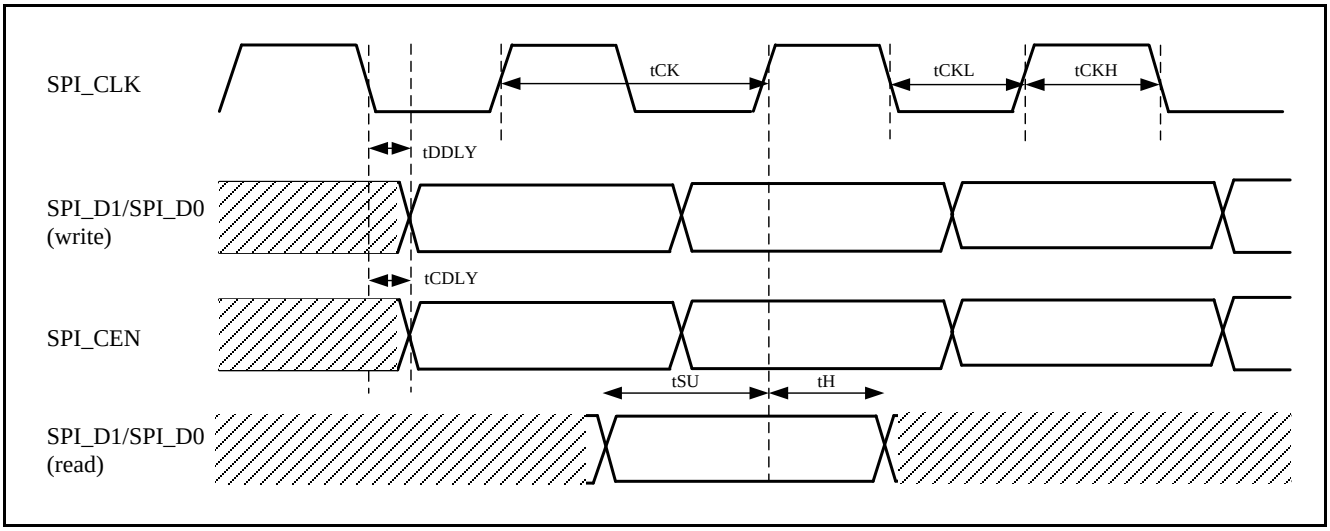
7.5. DC Characteristics

Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
TMDSTX Specification						
AVcc	Termination Supply Voltage		3.135		3.465	V
R_T	Termination Resistance		4.5		5.5	Ω
V_{OFF}	Single-ended standby(off) output voltage		AVcc-10mV		AVcc+10mV	V
V_{swing}	Single-ended output swing voltage		400		600	mV
V_H	Single-ended high level output voltage	Attached Sink supports <= 165MHz	AVcc-10mV		AVcc+10mV	V
		Attached Sink supports > 165MHz	AVcc-200mV		AVcc+10mV	V
V_H	Single-ended low level output voltage	Attached Sink supports <= 165MHz	AVcc-600mV		AVcc-400mV	V
		Attached Sink supports > 165MHz	AVcc-700mV		AVcc-400mV	V
MIPI Basic Specification						
AVDD	Analog operation Voltage		1.08	1.2	1.44	V
VDD	Core operation voltage		1.08	1.2	1.44	V
Temp	Operating temperature range		-40		125	℃
TStart	Power up/Power down time		1.08		20	uS
MIPI HS Mode						
VCMRX(DC)	Common-mode voltage HS receive mode		70		330	mV
VIDTH	Differential input high threshold				70	mV
VIDTL	Differential input low threshold		-70			mV
VIHHS	Single-ended input high voltage				460	mV
VILHS	Single-ended input low voltage		-40			mV
VOD	Differential voltage swing		70			mV
FCLK	Operating frequency		80		750	MHz
VTERM-EN	Single-ended threshold for HS termination enable				450	mV
ZID	Differential input impedance		80	100	125	Ω
MIPI LP Mode						
V_{IH}	Logic 1 input voltage		880			mV
V_{IL}	Logic 0 input voltage, not in ULP State				550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State				300	mV
V_{HYST}	Input hysteresis		25			mV
GPIO						
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2		5.5	V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL}	Low Output Current @ V_{OL} (max) (Port 1 ~ 8)	08:08mA	9.4	14.8	19.8	mA
I_{OL} 1	Low Output Current @ V_{OL} (max) (Port 0)	16:16mA	18.9	29.5	39.6	mA
I_{OH}	High Output Current @ V_{OL} (min) (Port 1 ~ 8)	08:08mA	14.0	28.7	48.2	mA
I_{OH} 1	High Output Current @ V_{OL} (min) (Port 0)	16:16mA	27.2	55.6	93.4	mA
Power Specification						

Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
I_{09} I_{12} I_{33}	Supply current @ SYSCLK = 202 MHz 0.9V supply current 1.2V supply current 3.3V supply current			? ? ?		mA
P_D	Power dissipation SYSCLK = 270 MHz Standby mode			?		mW

7.6. AC Characteristics

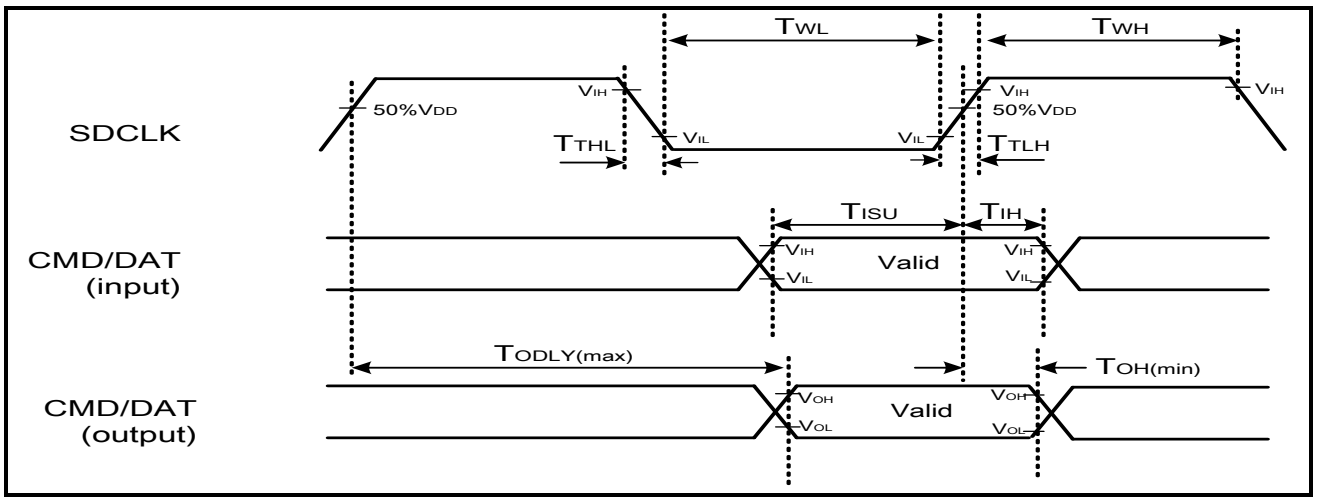
7.6.1. SPI Flash Specification



Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
tCK	Clock cycle for SPI Flash		20			ns
tCKH	Clock high-level width for SPI Flash		7			ns
tCKL	Clock low-level width for SPI Flash		7			ns
tDDLY	Write data output delay from SCK_FLASH Falling edge				5	ns
tCDLY	Control signals output delay from SCK_FLASH Falling edge				5	ns
tSU	Read data setup time		3			ns
tH	Read data hold time		3			ns

7.6.2. SD/SDIO Timing Diagrams

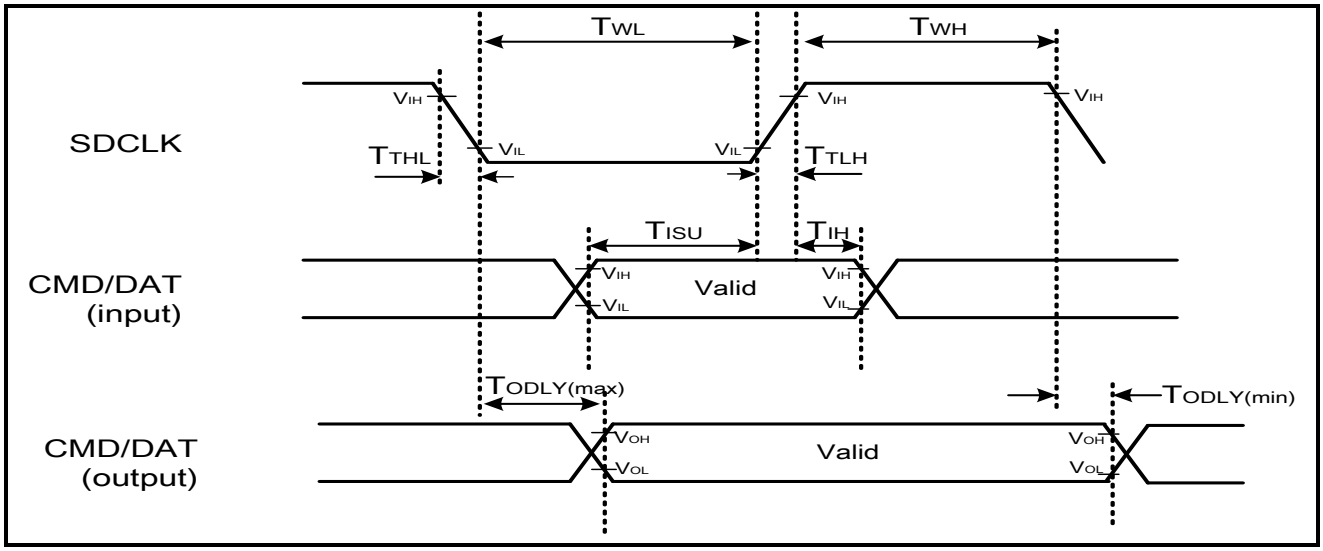
SD/SDIO High speed Mode



Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
V_{DD}	Supplu Voltage		2.7		3.6	V
V_{OH}	Output High Voltage	IOH = -2mA VDD min	0.75 * V_{DD}			V
V_{OL}	Output Low Voltage	IOL = 2mA VDD min			0.125 * V_{DD}	V
V_{IH}	Input High Voltage		0.625 * V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{SS}-0.3		0.25*V_{DD}	V
	Power Up Time	From 0V to VDD min			250	ms

Threshold Level for High Voltage

SD/SDIO Default speed Mode



Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
Clock CLK (All values are referred to min (VIH) and max (VIL))						
F_{PP}	Clock Frequency Data Transfer Mode	$C_{CARD} \leqq$ 10 pF (1 card)	0		25	
F_{OD}	Clock Frequency Identification Mode	$C_{CARD} \leqq$ 10 pF (1 card)	0[(1)]/100		400	
T_{WL}	Clock low time	$C_{CARD} \leqq$ 10 pF (1 card)	10			
T_{WH}	Clock high time	$C_{CARD} \leqq$ 10 pF (1 card)	10			
T_{TLH}	Clock rise time	$C_{CARD} \leqq$ 10 pF (1 card)			10	
T_{THL}	Clock fall time	$C_{CARD} \leqq$ 10 pF (1 card)			10	
Input CMD , DAT (referenced to CLK)						
T_{ISU}	Input set-up time	$C_{CARD} \leqq$ 10 pF (1 card)	5			ns
T_{IH}	Input hold time	$C_{CARD} \leqq$ 10 pF (1 card)	5			ns
Output CMD, DAT (referenced to CLK)						
T_{ODLY}	Output Delay time during Data Transfer Mode	$C_{CARD} \leqq$ 40 pF (1 card)	0		14	ns
T_{ODLY}	Output Delay time during Indentification Mode	$C_{CARD} \leqq$ 40 pF (1 card)	0		50	ns

Bus Timing - Parameters Values (Default Speed)

7.6.3. MIPI Timing Diagrams

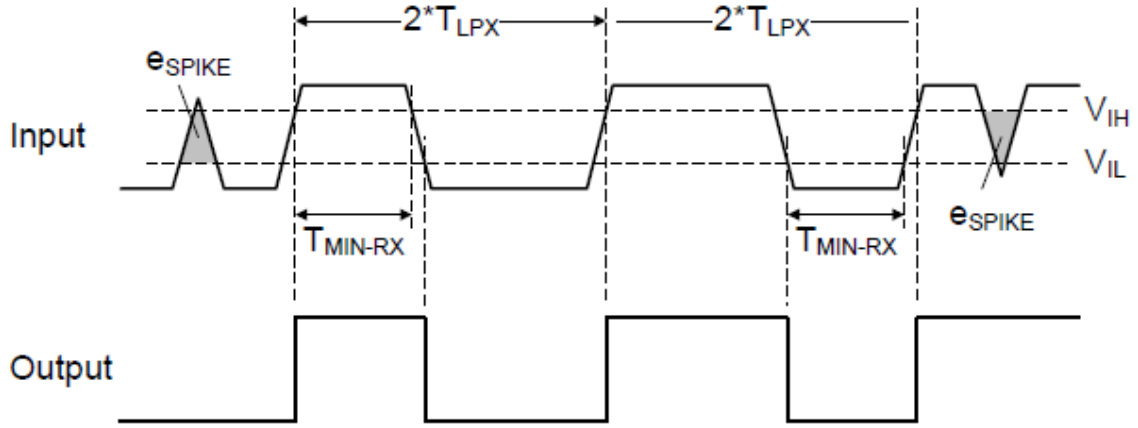


Fig.5.2.2 Input Glitch Rejection of Low-Power receiver

MIPI LP receiver AC specifications

Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
e_{SPIKE}	Input pulse rejection				300	V*ps
T_{MIN_RX}	Minimum pulse width response		20			ns
V_{INT}	Peak interference amplitude				200	mV
F_{INT}	Interference frequency		450		300	MHz

7.6.4. Ethernet Timing Diagrams

Serial Management Timing

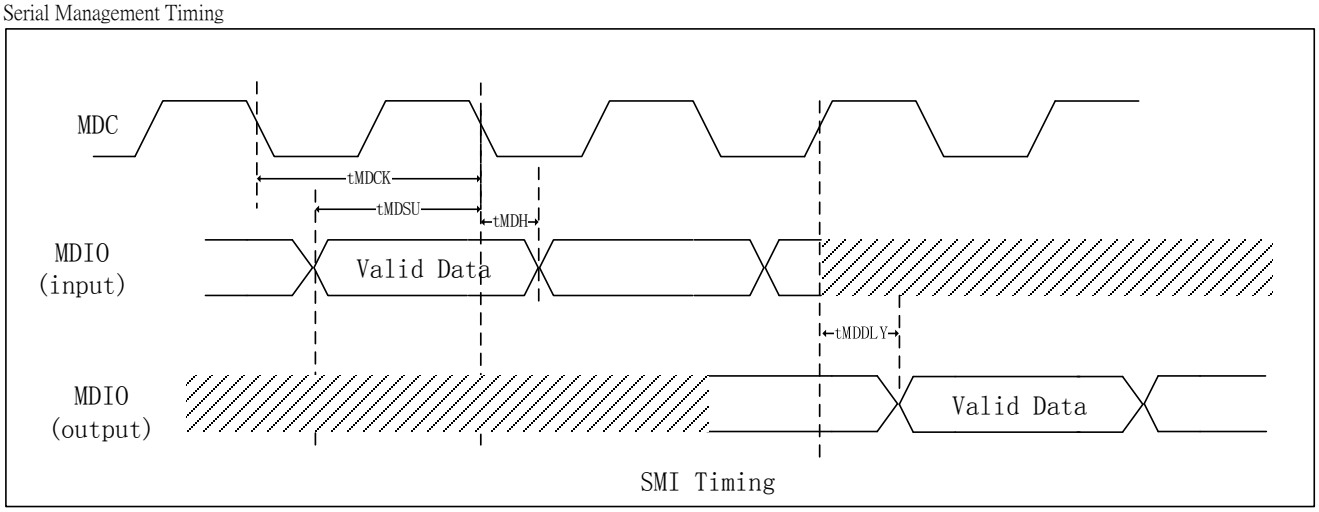


Figure: Ethernet SMI timing diagram

RMII Timing

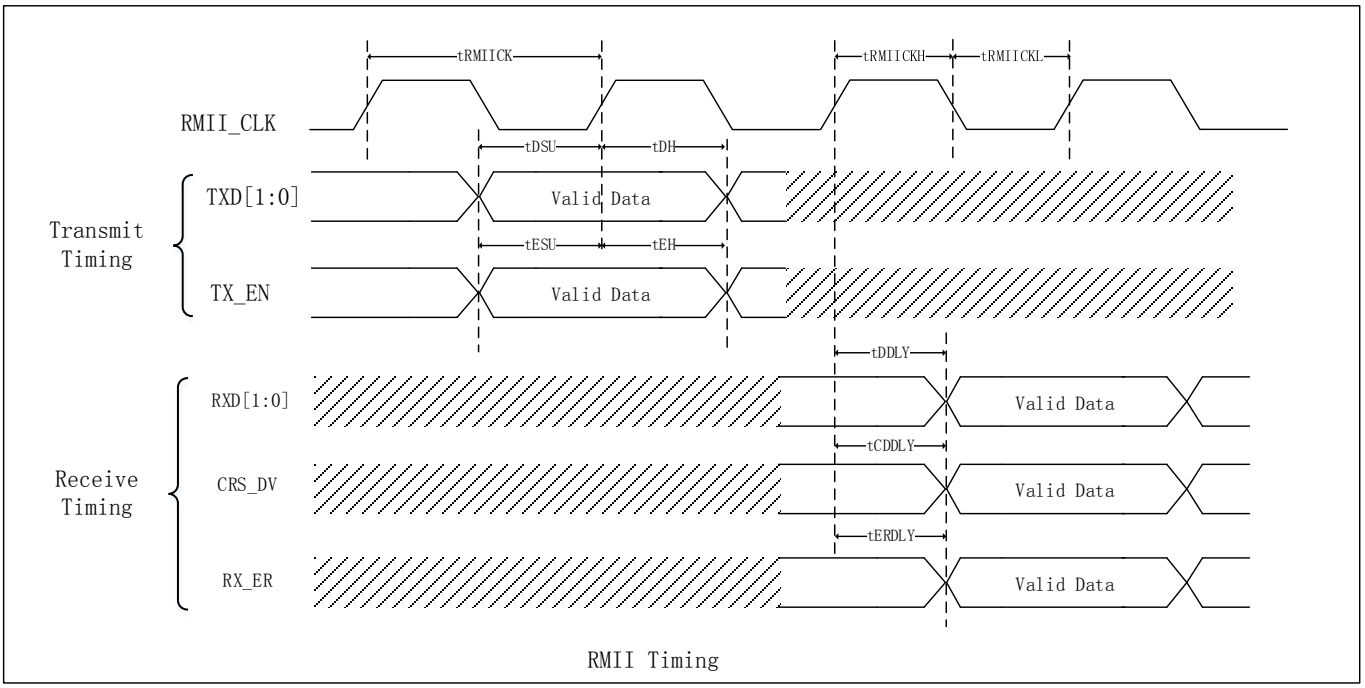


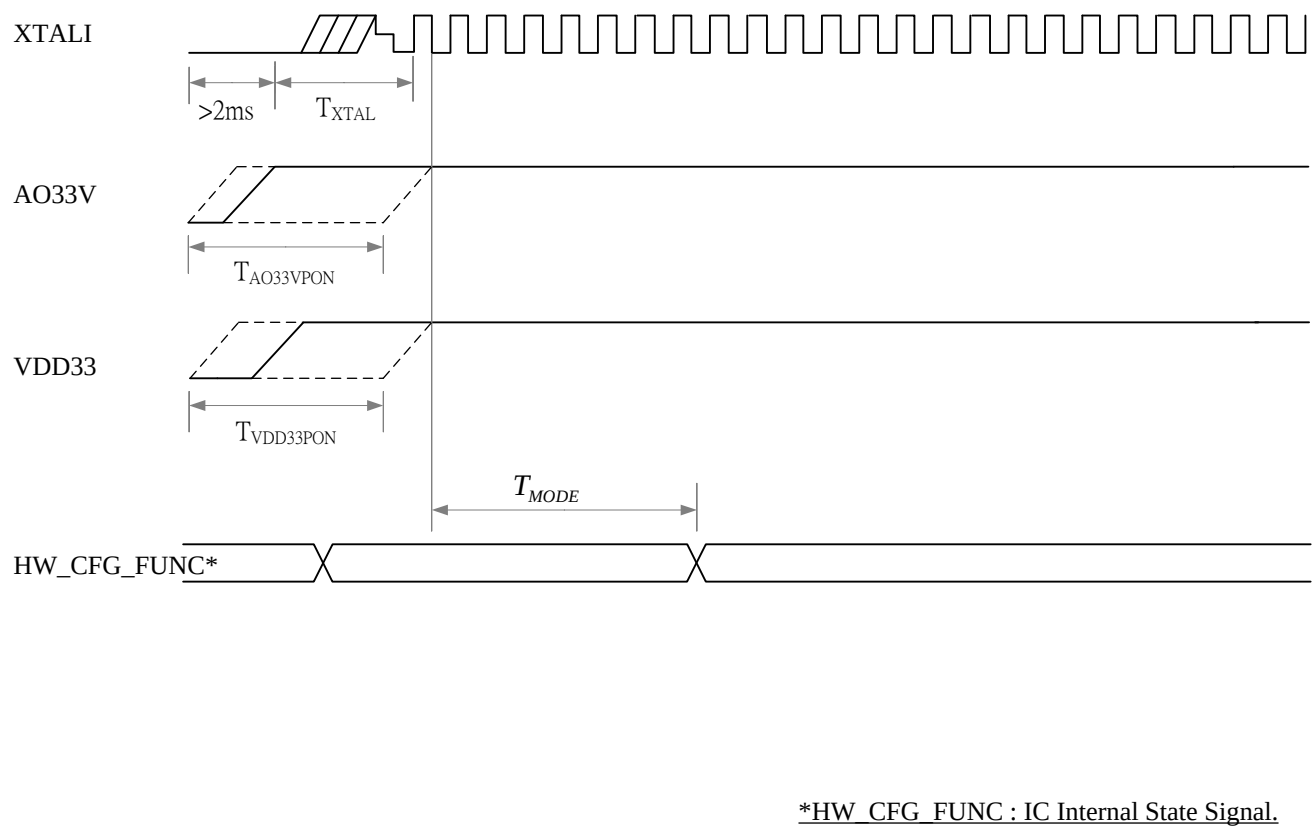
Figure: RMII Timing Diagram

Symbol	Parameter	Conditions	MIN.	Typ.	MAX.	Unit
tMDCK	Clock cycle for MDIO					ns
tMDCKH	Clock high-level width for MDIO					ns
tMDCKL	Clock low-level width for MDIO					ns
tMDDLY	MDC to MDIO (output) Delay Time					ns
tMDSU	MDIO (Input) to MDC Setup Time					ns
tMDH	MDIO (Input) to MDC Hold Time					ns
tRMIICK	Clock cycle for RMII					ns
tRMIICKH	Clock high-level width for RMII					ns
tRMIICKL	Clock low-level width for MDIO					ns
tDSU	TX_D[1:0] Setup to RMII Clock rising					ns
tDH	TX_D[1:0] Hold from RMII Clock rising					ns
tESU	TX_EN Setup to RMII Clock rising					ns
tEH	TX_EN Hold from RMII Clock rising					ns
tDDLY	RX_D[1:0] Delay from RMII Clock rising					ns
tCDDLY	CRS_DV Delay from RMII Clock rising					ns
tERDLY	RX_ER Delay from RMII Clock rising					ns

8.SYSTEM APPLICATIONS

8.1. Power On/Off Reset Sequence

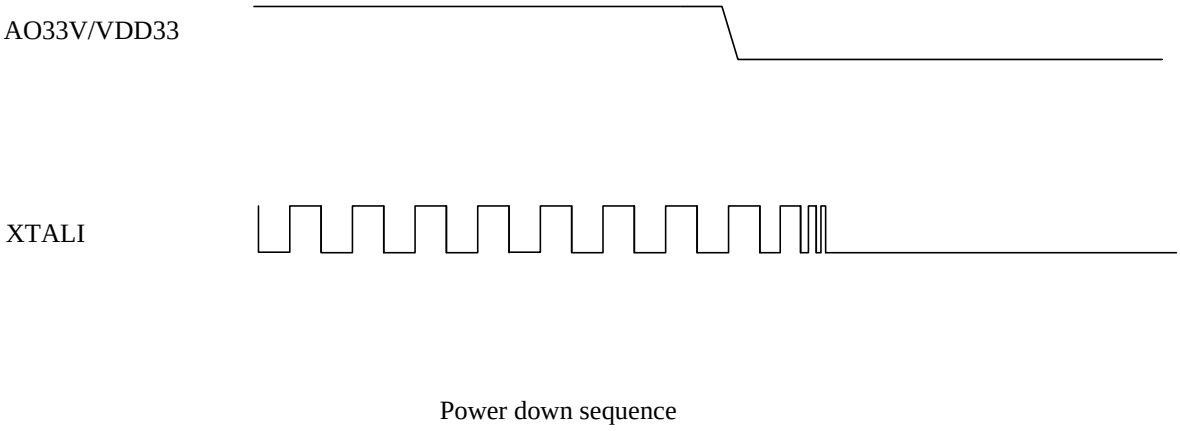
8.1.1. Power On Sequence



*HW_CFG_FUNC : IC Internal State Signal.

Parameter	Symbol	Min	Typ.	Max.	Units
XTAL clock output stable time	T_{XTAL}	5	-	-	us
AO33V power on timing range	$T_{AO33VPON}$	0	-	5	ms
VDD33 power on timing range	$T_{VDD33PON}$	0	-	5	ms
Operation mode configure time after AO33V and VDD33 power ready (include internal core power ramp up time and reset circuit time cost)	T_{MODE}	15	-	-	ms

8.1.2. Power Down Sequence



Power down sequence

8.1.3. Reset State

There are 3 physically event to trigger chip reset.

1. POR (Power On Reset)
2. External Reset
3. LVD (Low Voltage Detection)

- POR

The POR has 2 functions when AVDD33/DVDD12 becomes larger than the trip level. The first function is to give a reset pulse and the other function is to give a constant signal that tells whether the supply is on or off.

To have a better understanding of the functionality of the POR, see figure 7. In this figure a possible curve of AVDD33/DVDD12 is given with a dip at T3-T5 and a dip at T6-T7. At T0 the POR, porpulse, will start off with a '1' (= Voh). At T1 the detector passes through the triplevel, porconst becomes '1' after Thigh. A delay element will add an- other Tpulse before porpulse drops to '0'. This is done to make sure that the length of the generated detector pulse, porpulse, is large enough to reset asynchronous flip-flops. If the dip is too short (T7-T6 < Tlow) porpulse will not react and will stay low.

	PORPULSE	PORCONST
AVDD33/DVDD12 < Vtrip	'1'	'0'
AVDD33/DVDD12 > Vtrip	'0'	'1'

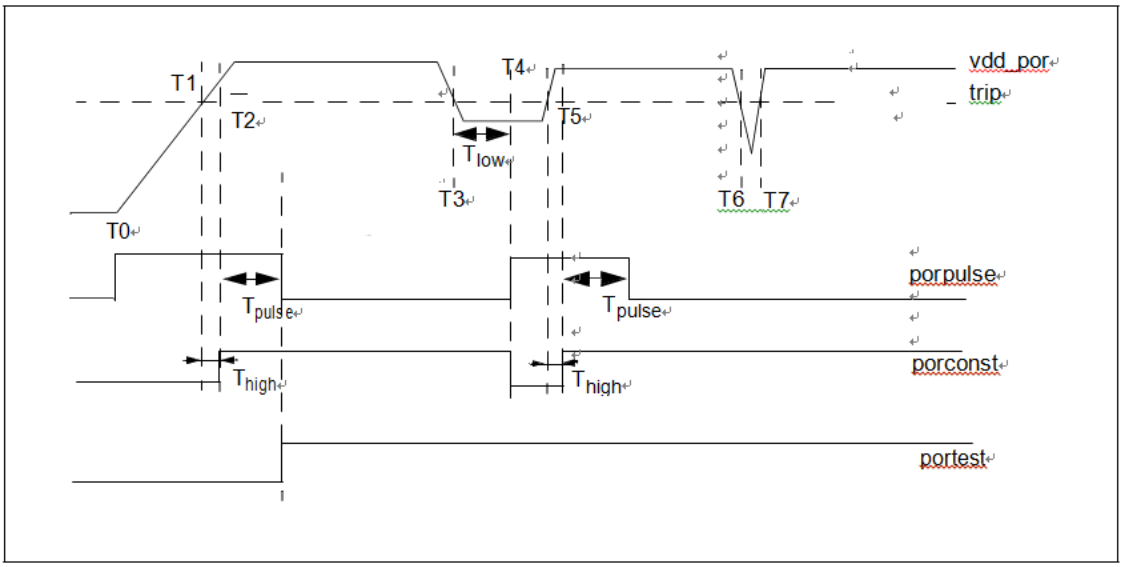
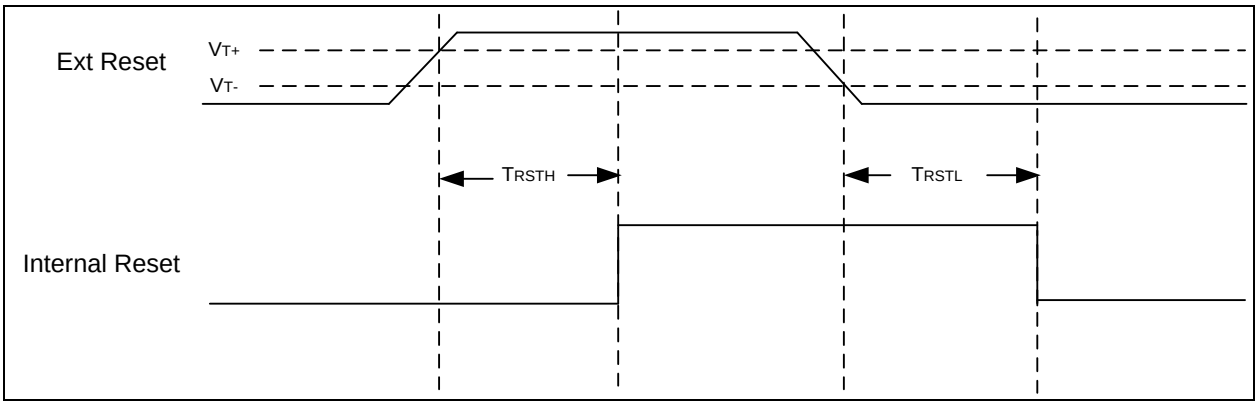


Figure 7. POR

PARAMETER	SYMBOL	MIN.	TYP.[1]	MAX.	UNIT
trip-level					
high trip-level	V_{trip_high}	**0.70**	**0.80**	**0.90**	V
low trip-level	V_{trip_low}	**0.65**	**0.75**	**0.85**	V
difference between high and low trip-level	HL_{trip_diff}	50	**70**	**100**	mV
timing					
time *vdd_por* has to be above V_{trip_high}[3] before *porconst* will be '1'	T_{high}			2	µs
time *vdd_por* has to be below V_{trip_low}[4] before *porconst* will be '0'	T_{low}			11	µs
time *porpulse* will be '1' after *vdd_por* > V_{trip_high}	T_{pulse}	200			ns

- External Reset

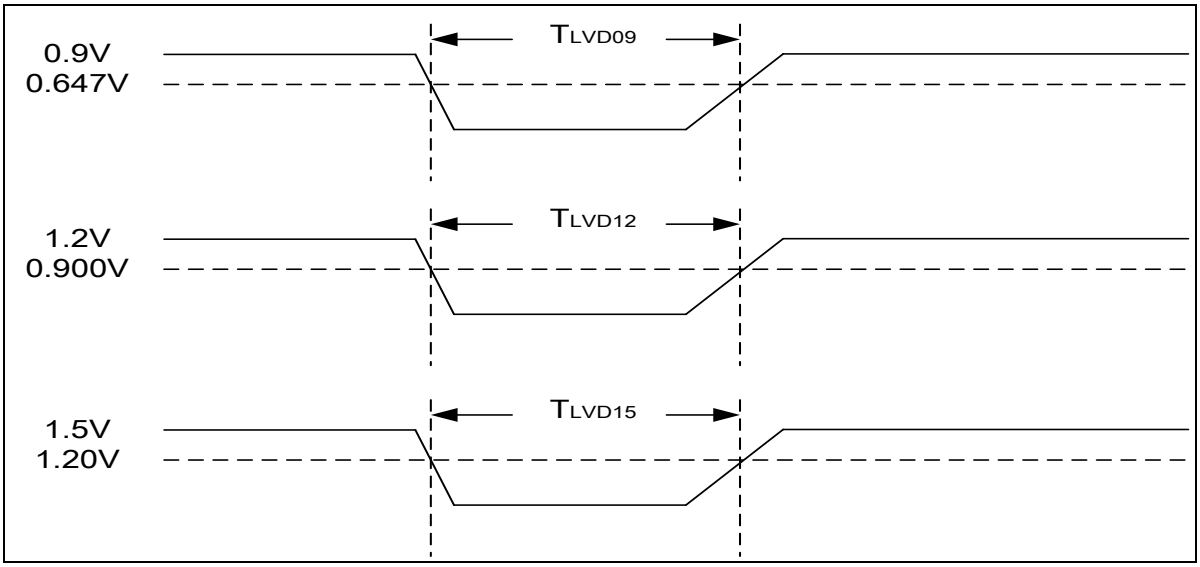
  External Reset connect to a button on PCB. Press the button can reset the whole chip to force the whole system restart. If external reset signal rising through V_{T+} and keep high time longer than T_{RSTH}, then internal reset signal deassert. If external reset signal falling through V_{T-}, and keep low time longer T_{RSTL}, then internal reset signal assert.



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
trip-level					
Low to High Threshold Point	V_{T+}	1.51	1.61	1.67	V
High to Low Threshold Point	V_{T-}	0.92	0.98	1.02	
timing					
Reset keep High Time	T_{RSTH}	1			µs
Reset keep Low Time	T_{RSTL}	1			µs

● LVD

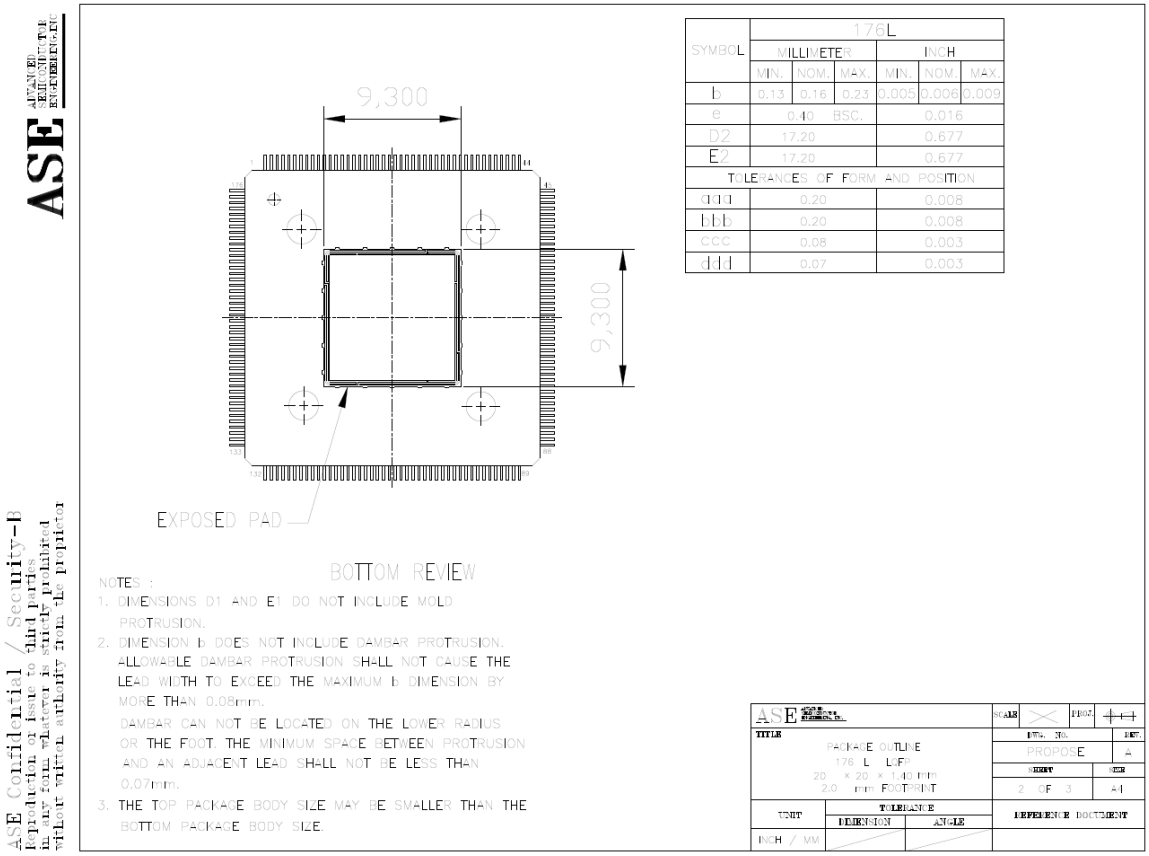
When 1.5V/ 1.2V/ 0.9V voltage lower than the setting reference voltage, reset signal will be assert to reset the whole chip.



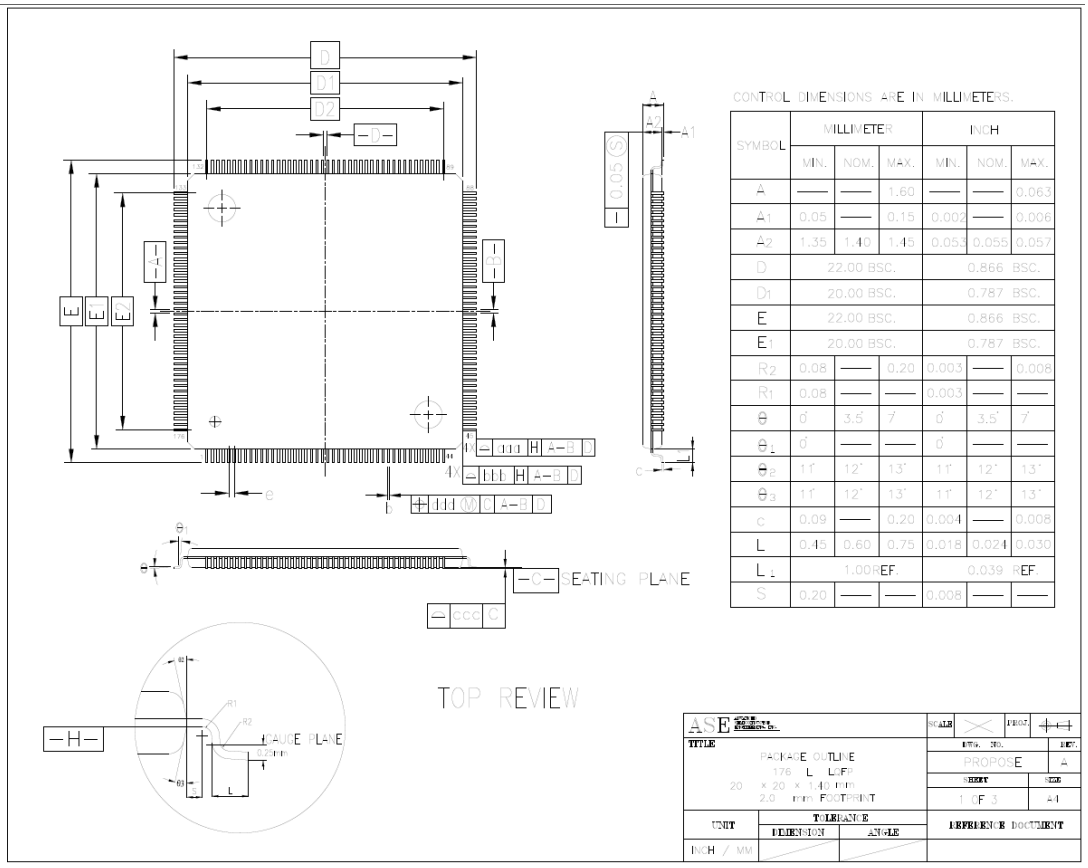
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
0.9V Low Voltage duration	T_{LVD09}			8	µs
1.2V Low Voltage duration	T_{LVD12}			8	µs
1.5V Low Voltage duration	T_{LVD15}			16	µs

9.PHYSICAL DIMENSION

9.1. Outline Dimensions 176-pin LQFP



SYMBOL	176L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016		
D2	17.20			0.677		
E2	17.20			0.677		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	——	——	1.60	——	——	0.063
A1	0.05	——	0.15	0.002	——	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	22.00 BSC.			0.866 BSC.		
E1	20.00 BSC.			0.787 BSC.		
R2	0.08	——	0.20	0.003	——	0.008
R1	0.08	——	——	0.003	——	——
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	——	——	0°	——	——
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	——	0.20	0.004	——	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF.			0.039 REF.		
S	0.20	——	——	0.008	——	——

ASE		SCALE: NONE	PROJ:
TITLE: PACKAGE OUTLINE 176L LQFP 20 x 20 x 1.40 mm 2.0 mm FOOTPRINT		DWG. NO.	REV.
		PROPOSE	A
		SHEET 1 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	

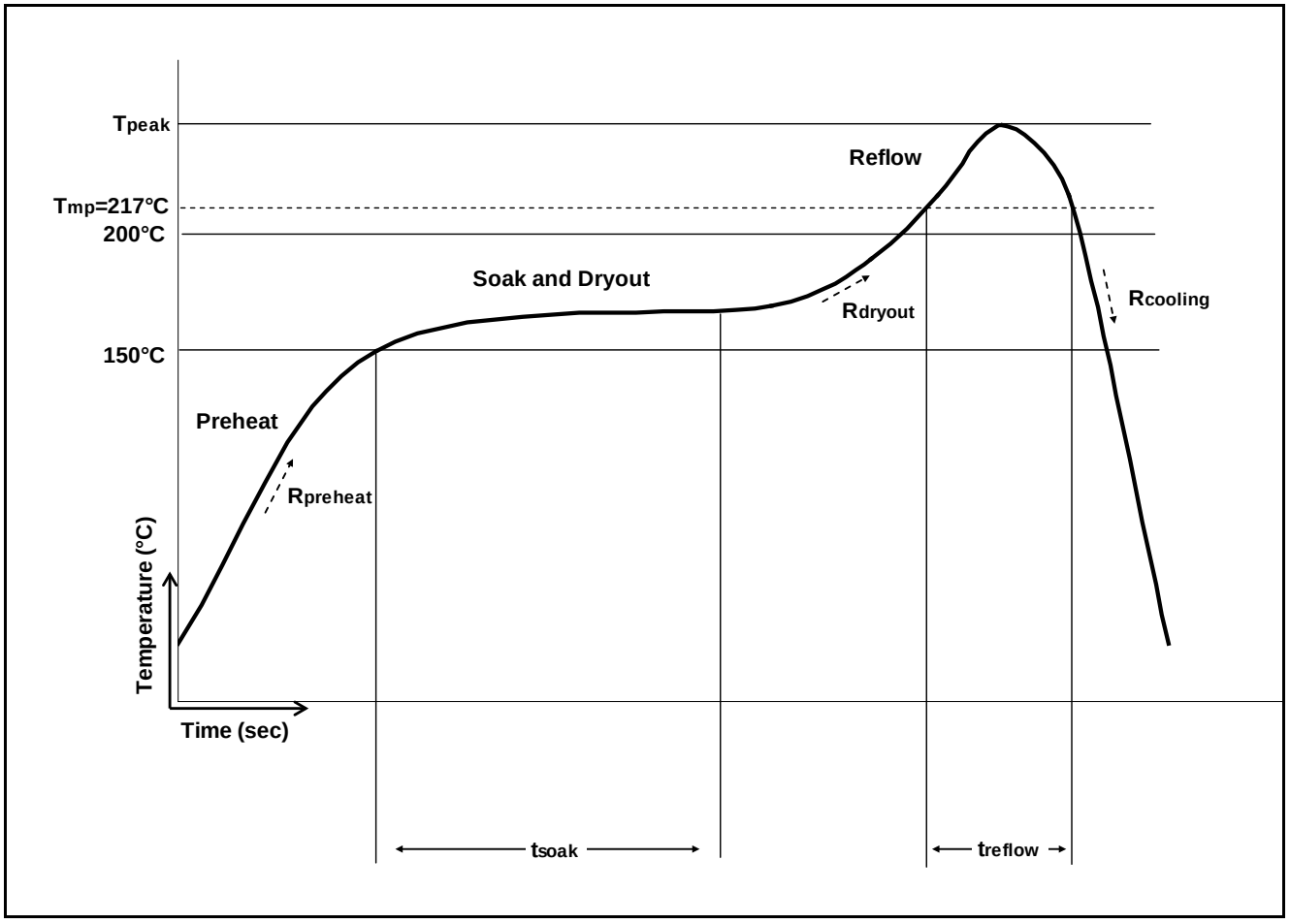
9.2. Recommended IR Reflow Profile

Recommended Solder Reflow Parameter Value

Parameter	Reference	Green Package
Average temperature gradient in preheating	Rpreheat	1-2°C /sec
Soak time	tsoak	60-90 sec
Temperature gradient in soak/dryout	Rdryout	2-3°C /sec
Time above Tmp (Melting Point), 217°C	treflow	40-60 sec
Peak temperature in reflow	Tpeak	217°C+20(min.) to 30°C(max.)
Temperature gradient in cooling	Rcooling	2-4°C /sec

Note: Sn/Ag/Cu are recommended for SMT application

Recommended Solder Reflow Profile



Note: The recommended solder reflow profile can meet IPC/JEDEC J-STD-020 requirement.

Note:

1. Compliance with the EU RoHS Directive
2. Material Recycling: Cu 30%

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
2018-9-19	0.1	Original	31
2019-4-18	0.1	Linux Computing Unit 取代 Super Control Unit Simple version TCON for LCD 320x240 application Security Boot	All
2019-4-19	0.2	● Rename to SP7021, ● add Plus1 story ● add block diagram	
2019-4-22	0.3	● Correct some typo	